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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,673	01/17/2002	David C. Chu	10020043-1	6492

7590 08/19/2003

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EXAMINER	
PRETLOW, DEMETRIUS R	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/052,673	CHU, DAVID C.
	Examiner	Art Unit
	Demetrius R. Pretlow	2863

-- The MAILING DATE of this communication appears on th cov r sh et with th correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,20,22 and 24* is/are rejected.

7)☒ Claim(s) *10,12-19,21,23 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 9, 10,21 and 25 are objected to because of the following informalities

In claim 9, it appears to be a lack of antecedent basis for one non-linearity parameter. Examiner is unclear as to whether this parameter is the same as the quasi-static non-linearity parameter.

In reference to claims 10,21 and 25 it appears to be a lack of antecedent basis for the temporal frequency. Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-9,11,20,22,24. are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. US 2003/0098981 in view of Demarest (US 6,597,459).

This is a provisional obviousness-type double patenting rejection.

10/052673 US 2003/0098981

1. A method for compensating non-linearity of the high-velocity type manifested in heterodyne interferometer position data, the method comprising: receiving a plurality of groups of digital position values; receiving a plurality of groups of digital phase values from a measurement channel; digitally processing a first group of the digital position values and digital phase values to generate a plurality of block data values; digitally processing the plurality of block data values to generate at least one quasi-static non-linearity parameter; and compensating a second group of the digital position values based on the at least one quasi-static non-linearity parameter.	1. A method for non-linearity compensating interferometer position data, the method comprising: receiving a plurality of groups of digital position values; digitally processing a first group of the digital position values to generate a plurality of data values; digitally processing the plurality of data values to generate at least one quasi-static non-linearity parameter; and compensating a second group of the digital position values based on the at least one quasi-static non-linearity parameter.
2. The method of claim 1, wherein the first group includes only measured digital position values and digital phase values.	2. The method of claim 1, wherein the first group includes only measured digital position values.
3. The method of claim 1, wherein the second group includes only measured digital position values.	3. The method of claim 1, wherein the second group includes only measured digital position values.
4. The method of claim 1, wherein the second group includes measured digital position values and extrapolated digital position values.	4. The method of claim 1, wherein the second group includes measured digital position values and extrapolated digital position values.
5. The method of claim 1, wherein each group of digital position values includes 320 position-data words.	5. The method of claim 1, wherein each group of digital position values includes 320 position-data words.
6. The method of claim 5, wherein the first group is processed in 10 blocks of 32 words each.	6. The method of claim 5, wherein the first group is processed in blocks of 32 words each.
7. The method of claim 6, wherein each position-data word is 32 bits.	7. The method of claim 6, wherein each position-data word is 32 bits.
8. The method of claim 1, wherein the at least one quasi-static non-linearity parameter is generated based on a block regression technique.	8. The method of claim 1, wherein the at least one quasi-static non-linearity parameter is generated based on a block regression technique.
9. The method of claim 1, wherein the at least one non-linearity parameter includes a non-linearity magnitude parameter and a non-linearity phase parameter.	9. The method of claim 1, wherein the at least one non-linearity parameter includes a non-linearity magnitude parameter and a non-linearity phase parameter.
10. The method of claims 1, wherein the temporal frequency of the nonlinearity being compensated is the difference between the measurement channel frequency and Doppler frequency.	10. The method of claim 1, wherein the temporal frequency of the non-linearity being compensated is the Doppler frequency.
11. A compensation system for compensating a high velocity type of nonlinearity in heterodyne interferometer position data, the	11. A compensation system for compensating interferometer position data, the system comprising: an input for receiving a plurality of groups of

system comprising:
a first input for receiving a plurality of groups of digital position values, each digital position value including a whole number portion and a fractional number portion;
a second input for receiving a plurality of groups of phase values from a measurement channel;
a digital position-data processor for digitally processing a first group of the digital position values and measurement channel phase values and generating a plurality of data values;
a digital data value processor for processing the plurality of data values and generating at least one non-linearity parameter; and
a digital compensator for compensating a second group of the digital position values based on the at least one non-linearity parameter.

12. The compensation system of claim 11, wherein the digital position-data processor comprises:
a cosine look-up table for providing cosine values corresponding to a fractional portion of the sum of received digital position values and measurement channel phase values;
a sine look-up table for providing sine values corresponding to a fractional portion of the sum of received digital position values and measurement channel phase values; a first plurality of arithmetic logic units (ALUs) for arithmetically processing the cosine values and the sine values, each ALU in the first plurality configured to output one of the plurality of data values based on the arithmetic processing; and a second plurality of ALUs for arithmetically processing received digital position values, each ALU in the second plurality configured to output one of the plurality of data values based on the arithmetic processing.

13. The compensation system of claim 12, wherein the digital position-data processor further comprises:
a plurality of registers coupled to the ALUs in the first and the second pluralities for storing the plurality of data values.

14. The compensation system of claim 13, wherein the digital position-data processor further comprises::
a counter coupled to the plurality of registers, the counter configured to cause the registers to store the plurality of data values at the end of each group of digital position values.

15. The compensation system of claim 14, wherein the counter is configured to generate signals for controlling operation of the first and the second plurality of ALUs.

digital position values, each digital position value including a whole number portion and a fractional number portion;

a digital position-data processor for digitally processing a first group of the digital position values and generating a plurality of data values;

a digital data value processor for processing the plurality of data values and generating at least one non-linearity parameter;

and a digital compensator for compensating a second group of the digital position values based on the at least one non-linearity parameter.

12. The compensation system of claim 11, wherein the digital position-data processor comprises:

a cosine look-up table coupled to the input for providing cosine values corresponding to the fractional portion of received digital position values;

a sine look-up table coupled to the input for providing sine values corresponding to the fractional portion of received digital position values; a first plurality of arithmetic logic units (ALUs) for arithmetically processing the cosine values and the sine values, each ALU in the first plurality configured to output one of the plurality of data values based on the arithmetic processing; and a second plurality of ALUs coupled to the input for arithmetically processing the digital position values in the first group, each ALU in the second plurality configured to output one of the plurality of data values based on the arithmetic processing.

13. The compensation system of claim 12, wherein the digital position-data processor further comprises: a plurality of registers coupled to the ALUs in the first and the second pluralities for storing the plurality of data values.

14. The compensation system of claim 13, wherein the digital position-data processor further comprises: a counter coupled to the plurality of registers, the counter configured to cause the registers to store the plurality of data values at the end of each group of digital position values.

15. The compensation system of claim 14, wherein the counter is configured to generate signals for controlling operation of the first and the second plurality of ALUs.

16. The compensation system of claim 12, and further comprising: a digital sequence generator for generating a plurality of digital sequences; and a third plurality of ALUs

16. The compensation system of claim 12, and further comprising:
a digital sequence generator for generating a plurality of digital sequences; and
a third plurality of ALUs coupled to the digital sequence generator for arithmetically processing the digital sequences, each ALU in the third plurality configured to output one of the plurality of data values based on the arithmetic processing.

17. The compensation system of claim 16, wherein the plurality of digital sequences include a constant sequence, a linearly increasing sequence with zero mean, and a quadratic sequence with zero mean, and wherein summation of one of the sequences results in a power-of-2 value, and summation of each of the remaining sequences results in a zero value.

18. The compensation system of claim 11, wherein each group of digital position values includes 320 position-data words, and wherein each group of measurement phase values includes 320 measurement phase words.

19. The compensation system of claim 18, wherein each position-data word is 32 bits.

20. The compensation system of claim 11, wherein the at least one nonlinearity parameter includes a non-linearity magnitude parameter and a nonlinearity phase parameter.

21. The compensation system of claim 11, wherein the temporal frequency of the non-linearity being compensated is the difference between the measurement channel frequency and Doppler frequency.

22. A displacement measuring heterodyne interferometer system comprising:
a light source for generating at least one light beam;
an interferometer for generating an optical measurement signal based on the at least one light beam;
a receiver for receiving the optical measurement signal and an optical reference signal, the receiver configured to generate an analog measurement signal based on the optical measurement signal and configured to generate an analog reference signal based on the optical reference signal; a controller for generating a plurality of groups of digital position values and measurement channel phase values based on the analog measurement signal and the analog reference signal; and at least one digital signal processor coupled to the controller for digitally processing each group of the digital position values and measurement channel phase values and generating a plurality of data values for each processed group, the at least one digital signal processor configured to ~~digitally process the plurality of data values~~ coupled to the digital sequence generator for arithmetically processing the digital sequences, each ALU in the third plurality configured to output one of the plurality of data values based on the arithmetic processing.

17. The compensation system of claim 16, wherein the plurality of digital sequences include a constant sequence, a linearly increasing sequence with zero mean, and a quadratic sequence with zero mean, and wherein summation of one of the sequences results in a power-of-2 value, and summation of each of the remaining sequences results in a zero value.

18. The compensation system of claim 11, wherein each group of digital position values includes 320 position-data words.

19. The compensation system of claim 17, wherein each position-data word is 32 bits.

20. The compensation system of claim 11, wherein the at least one non-linearity parameter includes a non-linearity magnitude parameter and a non-linearity phase parameter.

21. The compensation system of claim 11, wherein the temporal frequency of the non-linearity being compensated is the Doppler frequency.

22. A displacement measuring interferometer system comprising:

a light source for generating at least one light beam;

an interferometer for generating an optical measurement signal based on the at least one light beam;

a receiver for receiving the optical measurement signal and an optical reference signal, the receiver configured to generate an analog measurement signal based on the optical measurement signal and configured to generate an analog reference signal based on the optical reference signal; a controller for generating a plurality of groups of digital position values based on the analog measurement signal and the analog reference signal; and at least one digital signal processor coupled to the controller for digitally processing each group

digitally process the plurality of data values for each processed group to generate at least one nonlinearity parameter for each processed group, the at least one digital signal processor configured to non-linearity compensate digital position values based on the at least one non-linearity parameter, wherein the non-linearity being compensated is of a type occurring at relatively high velocities. 23. The interferometer system of claim 22, wherein each group of digital position values includes 320 position-data words and each group of measurement channel phase values includes a corresponding 320 data words. 24. The interferometer system of claim 22, wherein the at least one nonlinearity parameter includes a non-linearity magnitude parameter and a nonlinearity phase parameter. 25. The interferometer system of claim 22, wherein the temporal frequency of the non-linearity being compensated is the difference between the measurement signal frequency and Doppler frequency.	of the digital position values and generating a plurality of data values for each processed group, the at least one digital signal processor configured to digitally process the plurality of data values for each processed group to generate at least one non-linearity parameter for each processed group, the at least one digital signal processor configured to compensate digital position values based on the generated non-linearity parameters. 23. The interferometer system of claim 22, wherein each group of digital position values includes 320 position-data words. 24. The interferometer system of claim 22, wherein the at least one non-linearity parameter includes a non-linearity magnitude parameter and a non-linearity phase parameter. 25. The interferometer system of claim 22, wherein the temporal frequency of the non-linearity being compensated is the Doppler frequency.

4. Chu (US 2003/0098981) does not teach receiving a plurality of groups of digital phase values from a measurement channel, a second input for receiving a plurality of groups of digital phase values from a measurement channel, and digitally processing a first group of digital phase values.

Demarest teach receiving a plurality of groups of digital phase values from a measurement channel and digitally processing a first group of digital phase values. Note Demarest column 2, lines 16-27 and column 16, lines 30-49. Demarest teach a second input for receiving a plurality of groups of digital phase values from a measurement channel. Note Demarest column 12, lines 3-10.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the teaching of Demarest because it would allow full accuracy with dynamic multi-axis measurements. Note Demarest column 1, lines 62-63.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (703) 308-6722. The examiner can normally be reached on Monday - Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow, can be reached at (703) 308-3126. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Demetrius R. Pretlow Demetrius Pretlow 7/29/03

Patent Examiner

John Barlow
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